Listing of Claims:

1. (Canceled)

2. (Previously presented): A signal processing circuit processing a signal reproduced from a CD, comprising:

a CD-ROM decoder decoding incoming CD-ROM data by using a memory; and

an anti-shock controller causing a predetermined amount of incoming audio data to be stored in said memory, and reading and outputting the audio data from said memory, so that continuous output can be achieved even when the incoming audio data is interrupted; wherein

said CD-ROM decoder and said anti-shock controller access said memory; and

said memory is divided into an area used for decoding the CD-ROM data, and an area where the audio data is stored.

3-4. (Canceled)

5. (Previously presented): The circuit according to claim 7 further comprising an MP3 decoder decoding data, encoded in MP3 format and output from said CD-ROM decoder, in MP3 format.

6. (Previously presented): The circuit according to claim 5, further comprising a selection circuit selecting either an audio signal received from said anti-shock controller or the data encoded in MP3 format received from said MP3 decoder.

7. (Previously presented): A signal processing circuit processing a signal reproduced from a CD in which a CD-ROM data or CD-DA data is written, comprising:

a memory;

a CD-ROM decoder writing, when the CD from which the signal is to be reproduced is a CD-ROM, incoming CD-ROM data into said memory, and decoding said CD-ROM data while reading out the CD-ROM data from said memory;

an anti-shock controller causing, when the CD from which the signal is to be reproduced is a CD-DA, a predetermined amount of incoming CD-DA audio data to be stored in said memory, and reading and outputting the audio data from said memory, so that continuous output can be achieved even when the incoming audio data is interrupted;

a first arbiter generating an output signal for controlling said memory according to a request signal from said CD-ROM decoder;

a second arbiter generating an output signal for controlling said memory according to a request signal from said anti-shock controller;

a selection circuit selecting an output signal from said first or second arbiter; and

an MP3 decoder performing MP3 decoding on data encoded in MP3 format and output from said CD-ROM decoder;

wherein the first arbiter further performs read-out control in accordance with a read-out request signal from the MP3 decoder; and

an output signal from said first arbiter is selected by said selection circuit when the CD from which the signal is to be reproduced is a CD-ROM, and, when the CD from which the signal is to be reproduced is a CD-DA, an output signal from said second arbiter is selected by said selection circuit.

8. (Previously presented): A signal processing circuit as defined in Claim 7, further comprising

an access control circuit outputting to said memory, based on an output signal from said selection circuit, at least an address signal for said memory, a write-enable signal, and a read-enable signal.

9. (Canceled)

10. (Previously presented): A signal processing circuit as defined in Claim 7, wherein

when the CD from which the signal is to be reproduced is a CD-ROM, said CD-ROM decoder operates while said anti-shock controller stops operation, and, when the CD from which the signal is to be reproduced is a CD DA, said anti-shock controller operates while said CD-ROM decoder stops operation.

11. (Previously presented): A signal processing circuit as defined in Claim 8, wherein the access control circuit receives as an input address data from one of the CD-ROM decoder and the anti-shock controller.

12. (Previously presented): A signal processing circuit as defined in Claim 7, wherein one of the CD-DA data and the CD-ROM data is supplied to one of the anti-shock controller and the CD-ROM decoder via a data input/output circuit.

13. (Previously presented): A signal processing circuit as defined in Claim 8, wherein a subcode data and an error flag are further recorded in the memory.

14. (Previously presented): A signal processing circuit as defined in Claim 8, wherein the memory is a DRAM, and the access control circuit allows an RAS signal and a CAS signal to be output from a memory control circuit.

15. (Previously presented): A signal processing circuit as defined in Claim 8, wherein the signal processing circuit further comprises a refresh counter generating a refresh timing of the memory.

16. (Previously presented): A signal processing circuit as defined in Claim 7, wherein when switching between the CD-DA data and the CD-ROM data, data written before the switching is overwritten by data after the switching.

17. (Previously presented): A signal processing circuit as defined in Claim 7, wherein the MP3-encoded data is supplied to the MP3 decoder from the memory.

18. (Canceled)